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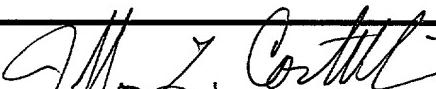
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REISSUE PATENT APPLICATION TRANSMITTAL		
ADDRESS TO: Assistant Commissioner for Patents Box Patent Application Washington, DC 20231	Attorney Docket No.	0756-2204
	First Named Inventor	Jun KOYAMA
	Original Patent Number	5,798,746
	Original Patent Issue Date (Month/Day/Year)	August 25, 1998
	Express Mail Label No.	
	Total Pages	22
APPLICATION FOR REISSUE OF: (check applicable box)		<input checked="" type="checkbox"/> Utility Patent <input type="checkbox"/> Design Patent <input type="checkbox"/> Plant Patent
APPLICATION ELEMENTS		ACCOMPANYING APPLICATION PARTS
<p>1. <input checked="" type="checkbox"/> Fee Transmittal Form (PTO/SB/56) (Submit an original, and a duplicate for fee processing)</p> <p>2. <input checked="" type="checkbox"/> Specification and Claims (amended, if appropriate)</p> <p>3. <input checked="" type="checkbox"/> Drawing(s) (proposed amendments, if appropriate)</p> <p>4. <input type="checkbox"/> Reissue Oath/Declaration (original or copy) (37 CFR 1.175) (PTO/SB/51 or 52)</p> <p>5. Original U.S. Patent</p> <p><input type="checkbox"/> Offer to Surrender Original Patent (37 CFR 1.178) (PTO/SB/53 or PTO/SB/54) or</p> <p><input type="checkbox"/> Ribboned Original Patent Grant <input type="checkbox"/> Affidavit/Declaration of Loss (PTO/SB/55)</p> <p>6. Original U.S. Patent currently assigned? <input type="checkbox"/> Yes <input type="checkbox"/> No</p> <p>(If Yes, check applicable box(es)) <input type="checkbox"/> Written Consent of all Assignees (PTO/SB/53 or 54) <input type="checkbox"/> 37 CFR 3.73(b) Statement <input type="checkbox"/> Power of Attorney</p>		
<p>7. <input type="checkbox"/> Transfer drawings from Patent File</p> <p>8. <input type="checkbox"/> Foreign Priority Claim (35 USC 119) (if applicable)</p> <p>9. <input checked="" type="checkbox"/> Information Disclosure Statement (IDS)/PTO-1449 <input type="checkbox"/> Copies of IDS Citations</p> <p>10. <input type="checkbox"/> English Translation of Reissue Oath/Declaration (if applicable)</p> <p>11. <input type="checkbox"/> Small Entity Statement(s) <input type="checkbox"/> Statement filed in prior application, Status still proper and desired</p> <p>12. <input type="checkbox"/> Preliminary Amendment</p> <p>13. <input checked="" type="checkbox"/> Return Receipt Postcard (MPEP 503) (Should be specifically itemized)</p> <p>14. <input type="checkbox"/> Other:</p>		
15. CORRESPONDENCE ADDRESS		
<input type="checkbox"/> Customer Number or Bar Code Label		or <input checked="" type="checkbox"/> Correspondence address below (Insert Customer No. or Attach bar code label here)
Name: Jeffrey L. Costellia Firm: NIXON PEABODY LLP Address: 8180 Greensboro Drive, Suite 800 City: McLean State: Virginia Zip Code: 22102 Country: U.S.A. Telephone (703) 790-9110 FAX (703) 883-0370		
16. SIGNATURE & DATE		
Name (Print/Type)	Jeffrey L. Costellia	Registration No. 35,483
Signature		

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<p>1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any over payments to Deposit Account No 19-2380 Deposit Account Name NIXON PEABODY LLP</p> <p>[X] Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17</p> <p>[] Charge the Issue Fee Set in 37 CFR 1.18 at the Mailing of the Notice of Allowance</p> <p>2. [X] Payment Enclosed [X] Check [] Money Order [] Other</p>				Fee Code	Fee (\$)	Fee Code	Fee (\$)	Fee Description	Fee Paid																																																																			
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<p>1. BASIC FILING FEE</p> <table border="1"> <thead> <tr> <th>Large Entity</th> <th>Small Entity</th> <th>Fee</th> <th>Fee</th> <th>Fee</th> <th>Fee</th> <th>Fee Description</th> <th>Fee Paid</th> </tr> <tr> <th>Code (\$)</th> <th>Code (\$)</th> <th>Fee (\$)</th> <th>Fee (\$)</th> <th>Fee (\$)</th> <th>Fee (\$)</th> <th></th> <th></th> </tr> </thead> <tbody> <tr> <td>101</td> <td>690</td> <td>201</td> <td>345</td> <td>Utility filing fee</td> <td>[]</td> <td></td> <td></td> </tr> <tr> <td>106</td> <td>310</td> <td>206</td> <td>155</td> <td>Design filing fee</td> <td>[]</td> <td></td> <td></td> </tr> <tr> <td>107</td> <td>480</td> <td>207</td> <td>240</td> <td>Plant filing fee</td> <td>[]</td> <td></td> <td></td> </tr> <tr> <td>108</td> <td>690</td> <td>208</td> <td>345</td> <td>Reissue filing fee</td> <td>[690.00]</td> <td></td> <td></td> </tr> <tr> <td>114</td> <td>150</td> <td>214</td> <td>75</td> <td>Provisional filing fee</td> <td>[]</td> <td></td> <td></td> </tr> <tr> <td colspan="4">SUBTOTAL (1)</td> <td colspan="4">[690.00]</td> </tr> </tbody> </table>				Large Entity	Small Entity	Fee	Fee	Fee	Fee	Fee Description	Fee Paid	Code (\$)	Code (\$)	Fee (\$)	Fee (\$)	Fee (\$)	Fee (\$)			101	690	201	345	Utility filing fee	[]			106	310	206	155	Design filing fee	[]			107	480	207	240	Plant filing fee	[]			108	690	208	345	Reissue filing fee	[690.00]			114	150	214	75	Provisional filing fee	[]			SUBTOTAL (1)				[690.00]				140	110	240	55					
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<p>2. EXTRA CLAIM FEES</p> <table border="1"> <thead> <tr> <th>Total Claims</th> <th>Extra Claims</th> <th>Fee from Below</th> <th>Fee Paid</th> </tr> <tr> <th></th> <th></th> <th>46 - 20** =</th> <th>26 X 18 =</th> </tr> <tr> <th>Independent Claims</th> <th></th> <th>11 - 3** =</th> <th>11 X 78 =</th> </tr> <tr> <th>Multiple Dependent Claims</th> <th></th> <th>-0-</th> <th>-0-</th> </tr> </thead> <tbody> <tr> <td colspan="4">**or number previously paid, if greater, For Reissues, see below</td> </tr> <tr> <td colspan="4"> <table border="1"> <thead> <tr> <th>Large Entry</th> <th>Small Entity</th> <th>Fee</th> <th>Fee</th> <th>Fee Description</th> </tr> <tr> <th>Code (\$)</th> <th>Code (\$)</th> <th>Fee (\$)</th> <th>Fee (\$)</th> <th></th> </tr> </thead> <tbody> <tr> <td>103</td> <td>18</td> <td>203</td> <td>9</td> <td>Claims in excess of 20</td> </tr> <tr> <td>102</td> <td>78</td> <td>202</td> <td>39</td> <td>Independent claims in excess of 3</td> </tr> <tr> <td>104</td> <td>260</td> <td>204</td> <td>130</td> <td>Multiple dependent claim</td> </tr> <tr> <td>109</td> <td>78</td> <td>209</td> <td>39</td> <td>**Reissue independent claims over original patent</td> </tr> <tr> <td>110</td> <td>18</td> <td>210</td> <td>9</td> <td>**Reissue claims in excess of 20 and over original patent</td> </tr> </tbody> </table> </td> </tr> <tr> <td colspan="4">SUBTOTAL (2)</td> <td colspan="4">[1326.00]</td> </tr> </tbody> </table>				Total Claims	Extra Claims	Fee from Below	Fee Paid			46 - 20** =	26 X 18 =	Independent Claims		11 - 3** =	11 X 78 =	Multiple Dependent Claims		-0-	-0-	**or number previously paid, if greater, For Reissues, see below				<table border="1"> <thead> <tr> <th>Large Entry</th> <th>Small Entity</th> <th>Fee</th> <th>Fee</th> <th>Fee Description</th> </tr> <tr> <th>Code (\$)</th> <th>Code (\$)</th> <th>Fee (\$)</th> <th>Fee (\$)</th> <th></th> </tr> </thead> <tbody> <tr> <td>103</td> <td>18</td> <td>203</td> <td>9</td> <td>Claims in excess of 20</td> </tr> <tr> <td>102</td> <td>78</td> <td>202</td> <td>39</td> <td>Independent claims in excess of 3</td> </tr> <tr> <td>104</td> <td>260</td> <td>204</td> <td>130</td> <td>Multiple dependent claim</td> </tr> <tr> <td>109</td> <td>78</td> <td>209</td> <td>39</td> <td>**Reissue independent claims over original patent</td> </tr> <tr> <td>110</td> <td>18</td> <td>210</td> <td>9</td> <td>**Reissue claims in excess of 20 and over original patent</td> </tr> </tbody> </table>				Large Entry	Small Entity	Fee	Fee	Fee Description	Code (\$)	Code (\$)	Fee (\$)	Fee (\$)		103	18	203	9	Claims in excess of 20	102	78	202	39	Independent claims in excess of 3	104	260	204	130	Multiple dependent claim	109	78	209	39	**Reissue independent claims over original patent	110	18	210	9	**Reissue claims in excess of 20 and over original patent	SUBTOTAL (2)				[1326.00]				146	760	246	380		
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LIQUID CRYSTAL DISPLAY DEVICE

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to an active matrix type liquid crystal display device, in particular, a liquid crystal display device for performing a digital gradation display.

2. Description of the Related Art

There is a conventional active matrix type liquid crystal display device for performing a digital gradation display, as described in Toshio Futami, Flat Panel Display '91, pp.173 to 180, 1990.

FIG.2 shows an example of an active matrix type liquid crystal display device. The active matrix type liquid crystal display device includes a pixel matrix portion 200, a signal line driving circuit 240 and a scanning line driving circuit 250.

In the pixel matrix portion 200, signal lines 201 to 203 and scanning lines 204 to 206 are arranged at a matrix form. Pixel thin film transistors (TFTs) 207 to 210 are arranged in intersection portions of the signal lines and the scanning lines. In each of the TFTs 207 to 210, a gate, a source and a drain are connected with the scanning line, the signal line and a pixel electrode, respectively. In general, since liquid crystals 211 to 214 arranged between the pixel electrodes and an opposite electrode cannot have a large capacitance value, storage capacitors 215 to 218 for storing charges are arranged in vicinity of the pixel electrodes.

When a voltage higher than a threshold voltage of the TFT is applied to the scanning line and the TFT is turned on, the drain and the source in the TFT are in a short circuit state. When a voltage on the signal line is applied to the pixel electrode, the liquid crystal and the storage capacitor are charged. On the other hand, when the TFT is turned off, since the drain and the source are in an open circuit state, charges in the liquid crystal and the storage capacitor are stored until the TFT is turned on.

FIG.3 shows an example of the 4-gradation signal line driving circuit 240. Note that the number of gradations is not limited to 4-gradations and the basic operation is the same. The signal line driving circuit 240 includes a clock signal input terminal 301, start pulse signal input terminals 302 and 303, a horizontal synchronizing signal input terminal 304, gradation (voltage) signal terminals 305 to 308, a signal line connection terminal 309, flip-flops (F/Fs) 310 to 313, latch circuits 314 and 315, a decoder 316, and TFTs 317 to 320.

Digital gradation signals as start pulse signals are supplied from the start pulse signal input terminals 302 and 303 to the flip-flops 310 and 311. Outputs of the flip-flops 310 and 311 are supplied to the flip-flops 312 and 313 and the latch circuits 314 and 315. Data supplied to the latch circuits 314 and 315 are stored for a desired period. The desired period is determined by a horizontal synchronizing signal supplied to the horizontal synchronizing signal input terminal 304. Output signals of the latch circuits 314 and 315 are supplied to the decoder 316. A digital signal of two bits supplied to the decoder 316 is converted into one of four voltage selection signals in the decoder 316. One of the TFTs 317 to 320 as switch transistors is selected in accordance with the converted voltage selection signal, and one of the voltages on the gradation signal lines 305a to 308a is supplied to the signal line 309.

Figs.4A shows an example of the scanning line driving circuit 250. The scanning line driving circuit 250 includes clocked invertor used circuits 410 to 412 (as shown in

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Figs.4B). NAND circuits 403 and 404 and inverter type buffers 405 and 406. The clocked inverter used circuit includes clocked invertors 420 and 421 operated by using a clock signal CK (as shown in FIG.4C) and an inverter 422.

5 The start pulse signal which synchronizes a vertical synchronizing signal is input from a start pulse signal input terminal 402, and the clock pulse signal which synchronizes the horizontal synchronizing signal is input from a clock pulse signal input terminal 401. Therefore, the scanning lines are driven sequentially through scanning line connection terminals 407 and 408.

In the conventional liquid crystal display, there are the following two problems.

(1) When a TFT is turned off, a leakage current flows 15 between a drain and a source, thereby to leak charges in pixels and to change a voltage applied to the liquid crystal.

FIG.5 shows a characteristic between a drain current I_d and a gate voltage G_{ds} in a commonly used N-channel TFT. From FIG.5, even if the gate voltage is negative, a current 20 flows into a drain and leakage of charge (discharge) produces by the current. In a P-channel TFT, the same discharge produces.

In general, since a pixel writing period (cycle) is 100 Hz 25 or less, a voltage (data) storage time in a pixel is 10 ms or more. Since it is necessary to obtain a long period of time as the storage time, a storage capacitor is usually arranged in parallel to a liquid crystal. Note that a total capacitance of the liquid crystal and the storage capacitor is about 0.1 to 0.2 30 pF.

When the storage time in the pixel is 16.6 ms (60 Hz), a voltage applied to the liquid crystal is 5 V, a storage rate 35 99%, a capacitance is 0.2 pF, admitting leakage current of a TFT is $5 \text{ V} \times (1 - 0.99) \times 0.2 \text{ pF}/16.6 \text{ ms} = 0.6 \text{ pA}$. Since it is difficult to obtain this value in consideration of a temperature range to be used and deviation of a characteristic of the TFT, charges in pixels leak and image quality deteriorates.

(2) In operation of a TFT, when a scanning line voltage is changed from a high voltage to a low voltage or from a low 40 voltage to a high voltage, the drain voltage is influenced to a scanning line voltage changing direction by ΔV calculated by the following equation in accordance with a capacitance between a gate and a drain in a TFT.

$$45 \quad \Delta V = V \times C_{gd} / (C_{gd} + C_{lc} + C_{stg})$$

where V is a deviation of a scanning line voltage, C_{gd} is a capacitance value between a gate and a drain in a TFT, C_{lc} is a capacitance value of a liquid crystal, C_{stg} is a capacitance value of a storage capacitor.

50 As a result, as shown in FIG. 6, a pixel voltage applied to a pixel electrode is shifted below, thereby to deteriorate a liquid crystal.

SUMMARY OF THE INVENTION

An object of the present invention is to solve the above 55 problems, and to provide a liquid crystal display wherein charges can be stored irrespective of a storage time and a storage voltage is not changed by a change of a scanning line voltage. The liquid crystal display device of the present invention is a time gradation display type. A voltage applied to a pixel corresponds to a binary value. One digital memory circuit is arranged for one pixel electrode and output of the digital memory circuit is connected with the pixel electrode.

65 In the present invention, a voltage on a signal line is supplied to the digital memory circuit in accordance with a scanning line signal and is stored for a desired period of

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time. Since the pixel electrode is connected with the output of the digital memory circuit, a high voltage or a low voltage in the digital memory circuit is supplied to the pixel electrode while the digital memory circuit is in a storage state.

According to the present invention, there is provided a liquid crystal display device comprising: first and second substrates each having an insulating surface; at least one pixel electrode arranged on the first substrate at a matrix form; an opposite electrode arranged on the second substrate; a liquid crystal arranged between the first and second substrates; and at least one digital memory circuit which is constructed by thin film transistors, wherein the digital memory circuit is connected with the pixel electrode and stores a voltage to be supplied to the pixel electrode.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 shows a signal line driving circuit and an active matrix circuit in a liquid crystal display device, according to an embodiment of the present invention;

FIG. 2 shows an example of an active matrix type liquid crystal display device;

FIG. 3 shows an example of a signal line driving circuit;

FIGS. 4A to 4C shows an example of a scanning line driving circuit;

FIG. 5 shows a characteristic between a drain current and a gate voltage in a commonly used N-channel TFT;

FIG. 6 shows an example of waveforms of voltages applied to a pixel electrode, an opposite electrode, and a gate of a TFT;

FIG. 7 is a view explaining a time gradation display manner;

FIG. 8 shows a pixel portion including a digital memory circuit, according to an embodiment of the present invention;

FIG. 9 shows a pixel portion including a digital memory circuit, according to another embodiment of the present invention; and

FIGS. 10A to 10C show waveforms of a digital memory circuit output voltage, an opposite electrode applying voltage, and a liquid crystal applying voltage.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 shows a signal line driving circuit and an active matrix circuit in a liquid crystal display device, according to an embodiment of the present invention. In a time gradation display manner, a half tone is displayed by changing between white and black in accordance with time elapse, as shown in FIG. 7.

The signal line driving circuit includes a clock signal input terminal 101, a start pulse signal input terminal 102, a horizontal synchronizing signal input terminal 103, scanning line connection terminals 104 and 105, signal line connection terminals 106 and 107, an opposite electrode connection terminal 108, flip-flops (F/Fs) 109 and 110, latch circuits 111 and 112, inverter type buffers 113 to 116, digital memory circuits 117 to 120, liquid crystals 121 to 124, pixel electrodes 130 to 133, and an opposite electrode 140. The liquid crystal 121 to 124 are arranged between the pixel electrodes 130 to 133 and the opposite electrode 140.

A digital gradation signal to be time-modulated as a start pulse signal is supplied from the start pulse signal input terminal 102 to the flip-flop 109. Outputs of the flip-flop 109 is supplied to the flip-flop 110 and the latch circuit 111.

Data supplied to the latch circuit 111 is stored for a desired period. The desired period is determined by a horizontal synchronizing signal supplied to the horizontal synchronizing signal input terminal 103. Output signals of the latch circuits 111 and 112 are supplied to the signal line connection terminals 106 and 107 through the inverter type buffers 113 to 116.

Data on the signal line connection terminals 106 and 107 are supplied to the digital memory circuits 117 to 120 arranged in vicinities of each of the pixel electrodes 130 to 133 in response to scanning line signals from the scanning line connection terminals 104 and 105. This storage state is held until a next scanning line signal is received.

FIG. 8 shows a pixel portion including a digital memory circuit, according to an embodiment of the present invention. The pixel portion includes a scanning line 801, a signal line 802, power source voltage terminals 803 and 804, an opposite electrode connection terminal 805, thin film transistors (TFTs) 806 to 810, and a liquid crystal 811.

In the digital memory circuit, an inverter constructed by the TFTs 807 and 808 and an inverter constructed by the TFTs 809 and 810 are integrated. When the TFT 806 is turned on, since the signal line 802 and the digital memory circuit is in a short circuit state, the signal line 802 is connected with the digital memory circuit and voltage data on the signal line 802 is stored in the digital memory circuit.

Since an output of the digital memory circuit is directly connected with the pixel electrode, a voltage on the pixel electrode is set to one of a high voltage and a low voltage as a power source voltage supplied from the power source voltage terminals 803 and 804. Therefore, Since a voltage on the pixel electrode is held by storing data in the digital memory circuit without storing a voltage into a capacitor, voltage deviation due to a leakage current of a pixel TFT and due to an off state of the TFT do not produce, thereby to improve an image quality.

Also, when a direct current voltage is applied to a liquid crystal element for a long period of time, since the liquid crystal is deteriorated, a voltage having the same amplitude as output of the digital memory circuit and a desired frequency such as a vertical synchronizing frequency is applied to an opposite electrode, so that a voltage applied to the liquid crystal is approximately zero on a time average. The voltage having the same amplitude as output of the digital memory circuit and a desired frequency such as a vertical synchronizing frequency can be used as the power source voltage of the digital memory circuit. This relationship is shown in FIGS. 10A to 10C. FIGS. 10A to 10C show waveforms of a digital memory circuit output voltage, an opposite electrode applying voltage, and a liquid crystal applying voltage.

FIG. 9 shows a pixel portion including a digital memory circuit, according to another embodiment of the present invention. The pixel portion includes a scanning line 901, a signal line 902, power source terminals 903 and 904, an opposite electrode connection terminal 905, thin film transistors (TFTs) 906, 908 and 910, resistors 907 and 909, and a liquid crystal 911. In the digital memory circuit, an inverter constructed by the TFTs 908 and 910 and the resistors 907 and 909 are used. The operation is the same as the digital memory circuit of FIG. 8. In this case, it is possible that a polarity of a TFT in a pixel matrix portion is only one type, that is, a P-channel type or an N-channel type.

As described above, time gradation display manner is used in the present invention. Since a digital memory circuit can be arranged every pixel electrode to supply a voltage to

each the pixel electrode, a voltage on the pixel electrode can be constant. Therefore, image quality can be improved.

What is claimed is:

1. A liquid crystal display device comprising:
first and second substrates each having an insulating surface;
at least one pixel electrode arranged on the first substrate at a matrix form;
an opposite electrode arranged on the second substrate;
a liquid crystal disposed between the first and second substrates; and
at least one digital memory circuit which is constructed by thin film transistors, wherein the digital memory circuit is connected with the pixel electrode and stores a binary information;
wherein a voltage is directly applied to said pixel electrode through said digital memory circuit based on said binary information,
wherein said liquid crystal display device includes a time gradation display device.

2. The device of claim 1 wherein a voltage having an amplitude equivalent to that of the voltage stored in the digital memory circuit is supplied to the opposite electrode.

3. The device of claim 1 wherein the number of pixel electrodes equals to the number of the digital memory circuit.

4. The device of claim 1 wherein the liquid crystal display device includes a digital gradation display device.

5. The device of claim 1 wherein the voltage includes one of a high voltage and a low voltage.

6. An active matrix display device having an electro-optical modulating layer disposed between a pair of substrates, said active matrix display device comprising:

- a plurality of column lines and a plurality of row lines supported by one of the substrates and defining a plurality of pixels in a matrix form;
- a plurality of pixel electrodes formed in said plurality of pixels and supported by said one of said substrates;
- a thin film transistor disposed in each of said pixels and electrically connected to one of said column lines and one of said row lines;
- a memory circuit disposed in each of said pixels and electrically connected to said thin film transistor, wherein said memory circuit stores an information output by said thin film transistor; and
- at least two signal lines electrically connected to said memory circuit and the corresponding pixel electrode, wherein different voltages are applied to said pixel electrode through said at least two signal lines based on the information stored by the corresponding memory circuit.

7. The active matrix display device of claim 6 further comprising an opposite electrode on the other of said substrates,

wherein an AC voltage having an amplitude equivalent to that of the voltages output of the memory circuit is supplied to the opposite electrode.

8. The active matrix display device of claim 6 wherein the number of pixel electrodes equals to the number of the memory circuit.

9. The active matrix display device of claim 6 wherein the active matrix display device includes a digital gradation display device.

10. The active matrix display device of claim 6 wherein the active matrix display device includes a time gradation display device.

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11. The active matrix display device of claim 6 wherein the different voltages include a high voltage and a low voltage.

12. An active matrix display device having an electro-optical modulating layer disposed between a pair of substrates, said active matrix display device comprising:

- a plurality of column lines and a plurality of row lines supported by one of the substrates and defining a plurality of pixels in a matrix form;
- 10 a plurality of pixel electrodes formed in said plurality of pixels and supported by said one of said substrates;
- a first thin film transistor disposed in each of said pixels and electrically connected to one of said column lines and one of said row lines;
- 15 a memory circuit disposed in each of said pixels and electrically connected to said first thin film transistor, wherein said memory circuit stores an information output by said first thin film transistor; and
- 20 at least two signal lines electrically connected to said memory circuit and the corresponding pixel electrode, wherein different voltages are applied to said pixel electrode through said at least two signal lines based on the information stored by the corresponding memory circuit, and
- 25 wherein said memory circuit comprises at least second and third thin film transistors,
- one of source or drain of the second thin film transistor being connected with one of said signal lines, a gate electrode of the third thin film transistor, and one of source or drain of the first thin film transistor,
- 30 the other of source or drain of the second transistor being connected with the other of said signal lines and one of source or drain of the third thin film transistor, and
- 35 a gate electrode of the second thin film transistor being connected with the other of source or drain of the third thin film transistor, one of said signal lines, and said electro-optical modulating layer.

13. The active matrix display device of claim 12 wherein 40 a voltage supplied to the electro-optical modulating layer is substantially zero on time average.

14. The active matrix display device of claim 12 wherein the number of pixel electrodes equals to the number of the memory circuit.

45 15. The active matrix display device of claim 12 wherein the active matrix display device includes a digital gradation display device.

16. The active matrix display device of claim 12 wherein the active matrix display device includes a time gradation display device.

50 17. The active matrix display device of claim 12 wherein the different voltages include a high voltage and a low voltage.

18. An active matrix display device having an electro-optical modulating layer disposed between a pair of substrates, said active matrix display device comprising:

- a plurality of column lines and a plurality of row lines supported by one of the substrates and defining a plurality of pixels in a matrix form;
- 60 a plurality of pixel electrodes formed in said plurality of pixels and supported by said one of said substrates;
- a first thin film transistor disposed in each of said pixels and electrically connected to one of said column lines and one of said row lines;
- 65 a memory circuit disposed in each of said pixels and electrically connected to said first thin film transistor.

wherein said memory circuit stores an information output by said first thin film transistor; and

at least two signal lines electrically connected to said memory circuit and the corresponding pixel electrode, wherein different voltages are applied to said pixel electrode through said at least two signal lines based on the information stored by the corresponding memory circuit, and

wherein said memory circuit comprises at least two invertors, said invertors comprising at least two thin film transistors and being connected with said signal lines.

19. The active matrix display device of claim 18 wherein the number of pixel electrodes equals to the number of the memory circuit.

20. The active matrix display device of claim 18 wherein the active matrix display device includes a digital gradation display device.

21. The active matrix display device of claim 18 wherein the active matrix display device includes a time gradation display device.

22. The active matrix display device of claim 18 wherein the different voltages include a high voltage and a low voltage.

23. The active matrix display device of claim 18 further comprising an opposite electrode on the other of said substrates,

wherein an AC voltage having an amplitude equivalent to that of the voltages output of the memory circuit is supplied to the opposite electrode.

24. An active matrix display device having an electro-optical modulating layer disposed between a pair of substrate, said active matrix display device comprising:

a plurality of column lines and a plurality of row lines supported by one of the substrates and defining a plurality of pixels in a matrix form;

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- a plurality of pixel electrodes formed in said plurality of pixels and supported by said one of said substrates;
- 5 first thin film transistor disposed in each of said pixels and electrically connected to one of said column lines and one of said row lines;
- 10 a memory circuit disposed in each of said pixels and electrically connected to said first thin film transistor, wherein said memory circuit stores an information output by said first thin film transistor; and
- 15 at least two signal lines electrically connected to said memory circuit and the corresponding pixel electrode, wherein different voltages are applied to said pixel electrode through said at least two signal lines based on the information stored by the corresponding memory circuit, and
- wherein said memory circuit comprises at least two thin film transistors, having a same conductivity type.
- 20 25. The active matrix display device of claim 24 wherein a voltage supplied to the electro-optical modulating layer is substantially zero on time average.
- 25 26. The active matrix display device of claim 24 wherein the number of pixel electrodes equals to the number of the memory circuit.
27. The active matrix display device of claim 24 wherein the active matrix display device includes a digital gradation display device.
- 30 28. The active matrix display device of claim 24 wherein the active matrix display device includes a time gradation display device.
- 35 29. The active matrix display device of claim 24 wherein the different voltages include a high voltage and a low voltage.

30. A method of operating an active matrix display device comprising the steps of:

storing a data in a memory circuit provided at one pixel; and
supplying a voltage to a pixel electrode of said pixel in accordance with the data stored in said memory circuit,

wherein said memory circuit comprises at least first and second inverters, each inverter comprising one p-channel type thin film transistor and one n-channel type thin film transistor formed over a substrate.

31. The method according to claim 30 wherein an output terminal of said memory circuit is connected to said pixel electrode.

32. A method of operating an active matrix display device comprising the steps of:

supplying a data through a switching thin film transistor provided at one pixel to a memory circuit;

storing said data in a memory circuit provided at said pixel;

supplying a voltage to a pixel electrode of said pixel in accordance with the data stored in said memory circuit,

wherein said memory circuit comprises at least first and second inverters, each inverter comprising one p-channel type thin film transistor and one n-channel type thin film transistor formed over a substrate.

33. The method according to claim 32 wherein an output terminal of said memory circuit is connected to said pixel electrode.

34. A method of operating an active matrix display device comprising the steps of:

storing a data in a memory circuit provided at one pixel; and

supplying a voltage to a pixel electrode of said pixel in accordance with the data stored in said memory circuit,

wherein said memory circuit comprises at least first and second inverters, each inverter comprising one p-channel type thin film transistor and one n-channel type thin film transistor formed over a substrate, and wherein a power source voltage of said memory circuit is an alternating voltage.

35. The method according to claim 34 wherein an output terminal of said memory circuit is connected to said pixel electrode.

36. A method of operating an active matrix display device comprising the steps of:

supplying a data through a switching thin film transistor provided at one pixel to a memory circuit;

storing said data in a memory circuit provided at said pixel;

supplying a voltage to a pixel electrode of said pixel in accordance with the data stored in said memory circuit,

wherein said memory circuit comprises at least first and second inverters, each inverter comprising one p-channel type thin film transistor and one n-channel type thin film transistor formed over a substrate, and wherein a power source voltage of said memory circuit is an alternating voltage.

37. A method of operating an active matrix display device comprising the steps of:

storing a data in a memory circuit provided at one pixel; and

supplying one of high and low voltages to a pixel electrode of said pixel in accordance with the data stored in said memory circuit,

wherein said memory circuit comprises at least first and second inverters, each inverter comprising one p-channel type thin film transistor and one n-channel type thin film transistor formed over a substrate.

38. The method according to claim 37 wherein an output terminal of said memory circuit is connected to said pixel electrode.

39. An active matrix display device comprising:

a substrate having an insulating surface;

at least one signal line and at least one scanning line extending across said signal line over said substrate wherein a pixel is defined by said signal line and said scanning line;

a switching element disposed at an intersection of said signal line and said scanning line;

a memory circuit electronically connected to said switching element; and

a pixel electrode disposed in said pixel,

wherein said memory circuit comprises at least first and second inverters, each inverter comprising one p-channel type thin film transistor and one n-channel type thin film transistor formed over a substrate.

40. An active matrix display device according to claim 39 wherein an output terminal of said memory circuit is connected to said pixel electrode.

41. An active matrix display device according to claim 39 wherein said display device is a liquid crystal device.

42. The method according to claim 30 wherein said display device is a liquid crystal device.

43. The method according to claim 32 wherein said display device is a liquid crystal device.

44. The method according to claim 34 wherein said display device is a liquid crystal device.

45. The method according to claim 36 wherein said display device is a liquid crystal device.

46. The method according to claim 37 wherein said display device is a liquid crystal device.

ABSTRACT

In an active matrix type liquid crystal display device, a time gradation display manner for performing time gradation display is used. A digital gradation (voltage) signal on a signal line is supplied to the digital memory circuit arranged in vicinity of each pixel electrode and stored therein for a desired period of time. This storage state is held until next scanning is started. A high voltage or a low voltage supplied as a power source voltage of the digital memory circuit is applied to a pixel electrode while the digital memory circuit is in a storage state, so that a desired voltage is stably applied to the pixel electrode.

FIG. 1

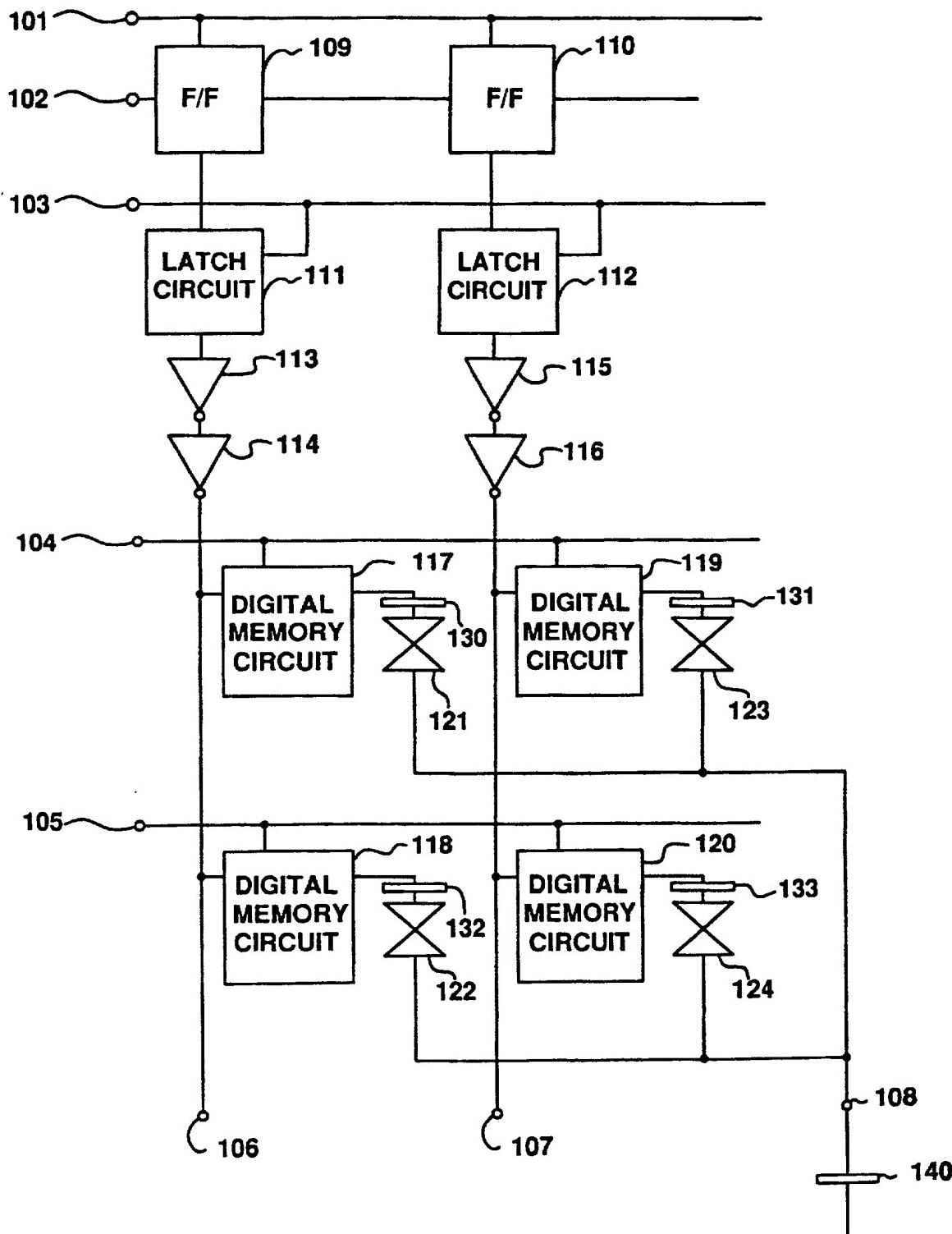


FIG. 2
PRIOR ART

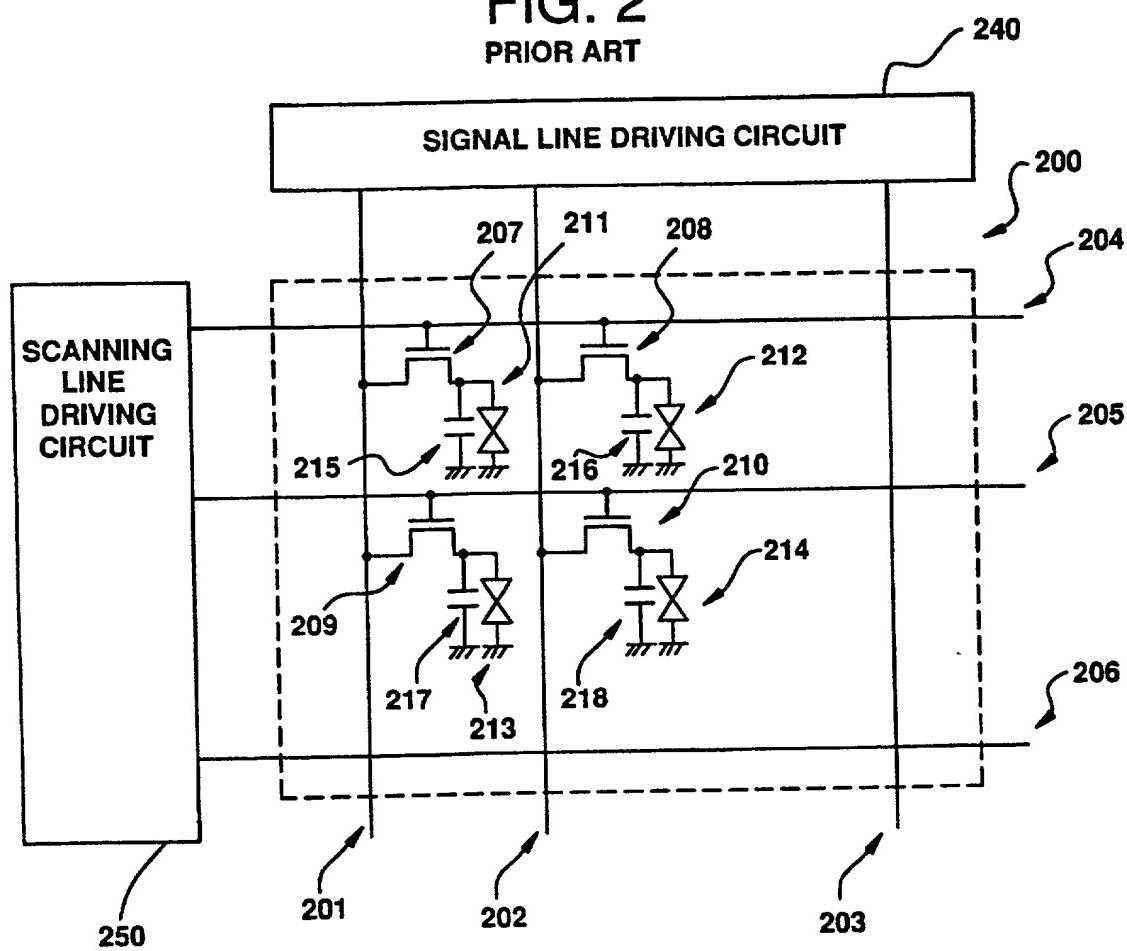


FIG. 3
PRIOR ART

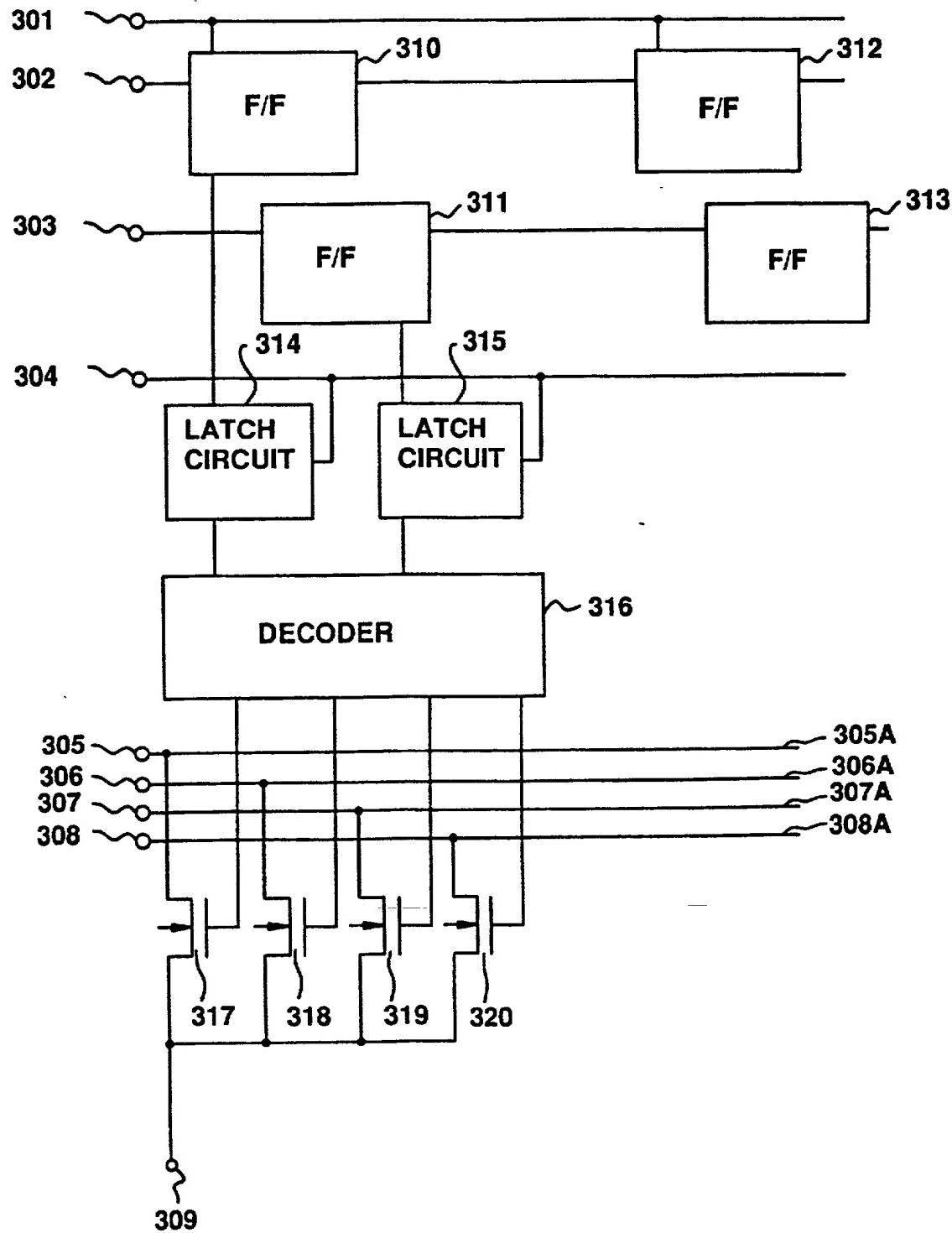


FIG. 4A

PRIOR ART

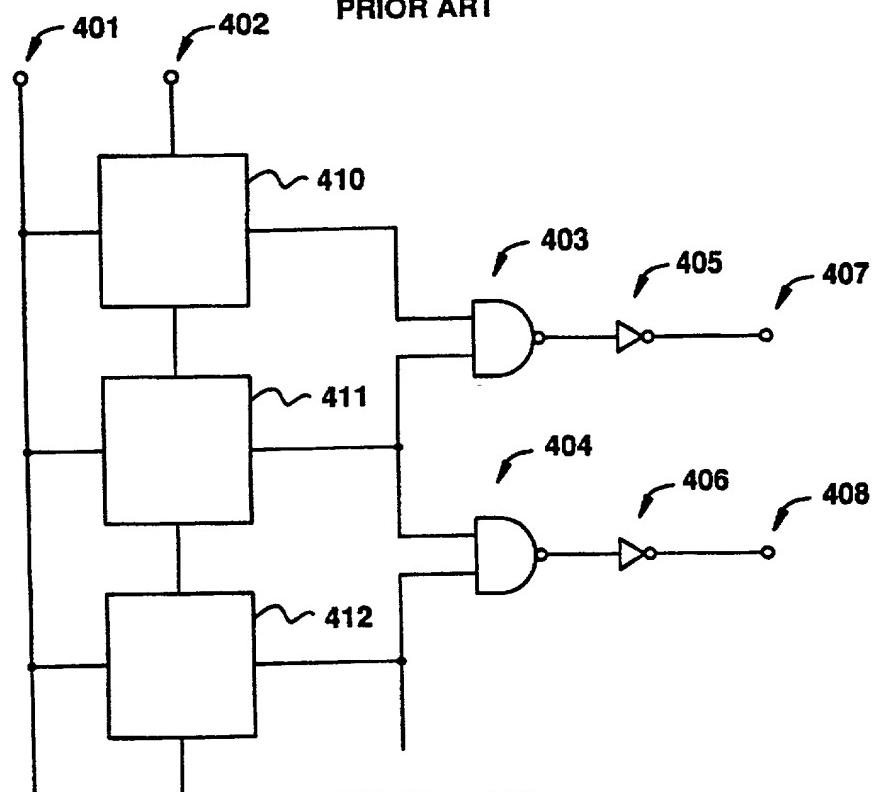


FIG. 4B

PRIOR ART

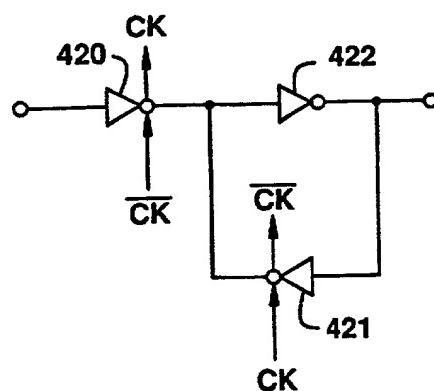
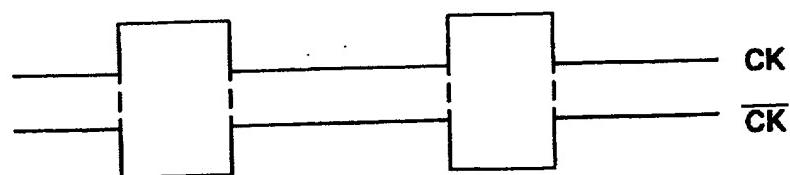


FIG. 4C

PRIOR ART



DRAIN
CURRENT
 $\log I_d$

FIG. 5
PRIOR ART

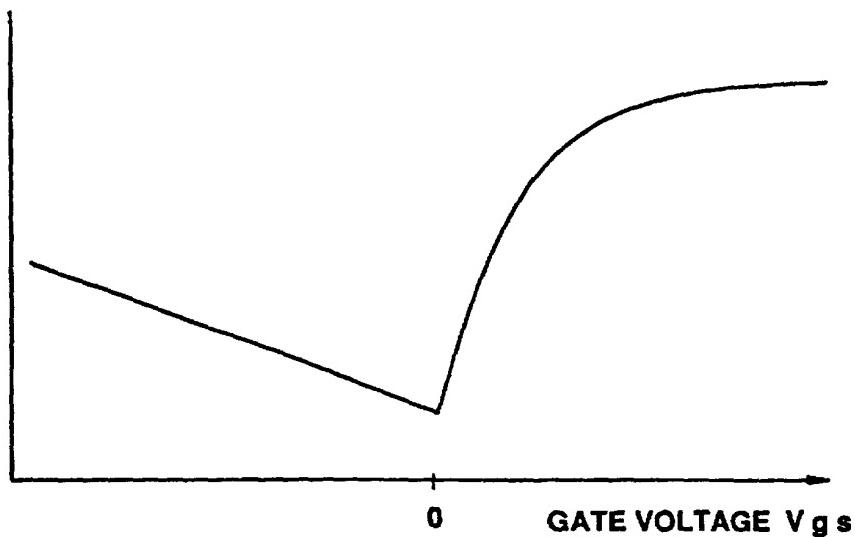


FIG. 6
PRIOR ART

VOLTAGE

ΔV

OPPOSITE
ELECTRODE
VOLTAGE

TIME

— PIXEL VOLTAGE

— TFT GATE VOLTAGE

FIG. 7

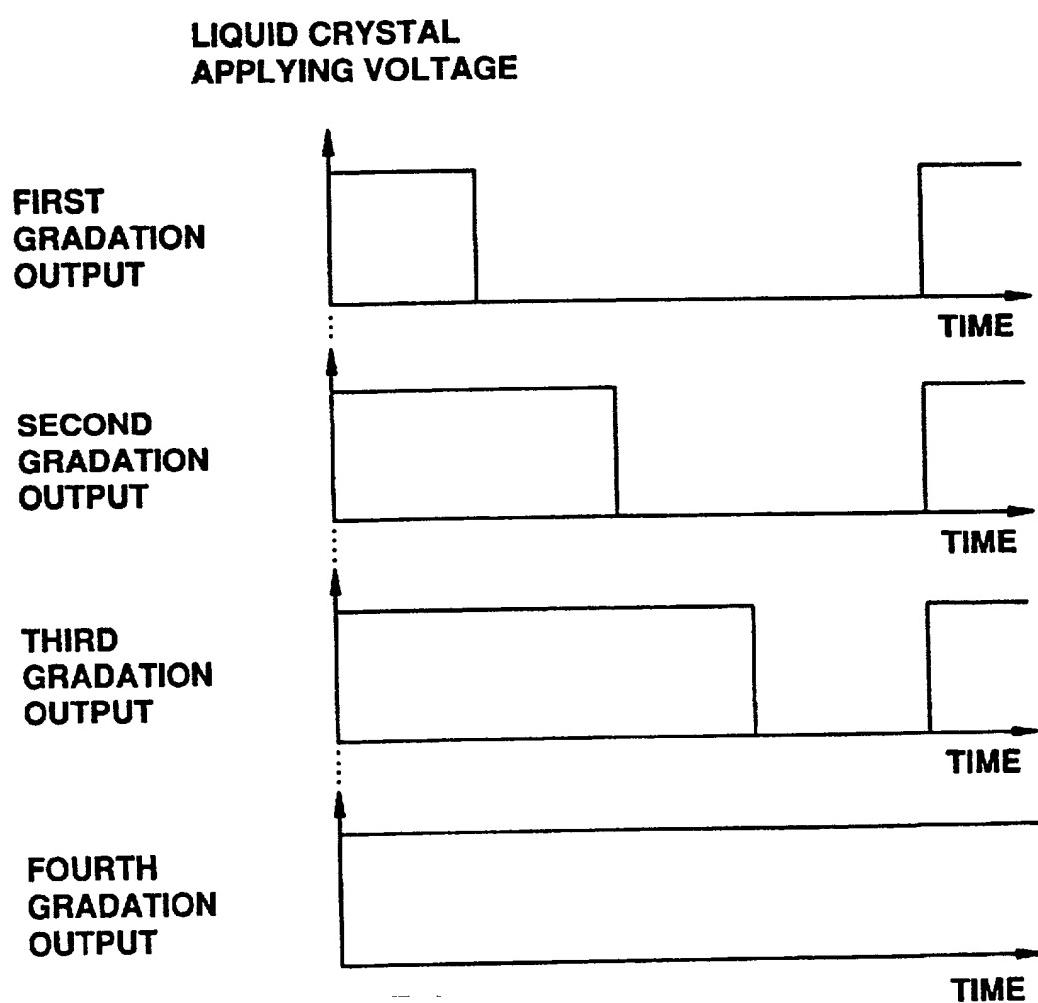


FIG. 8

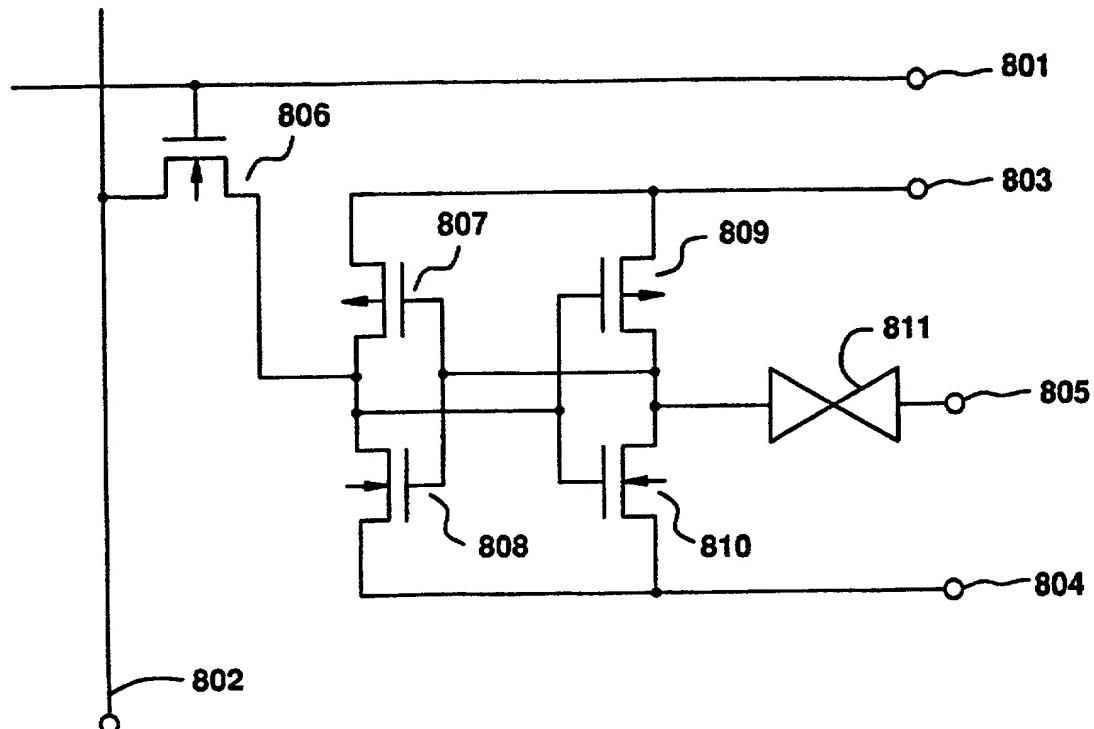
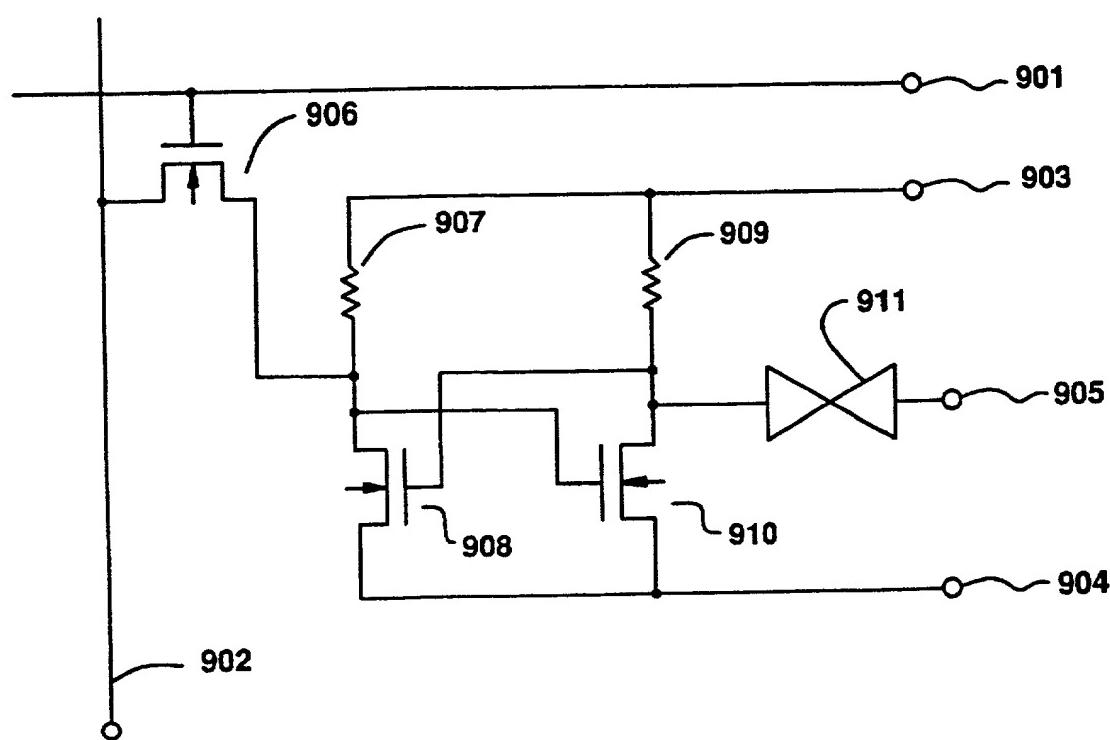
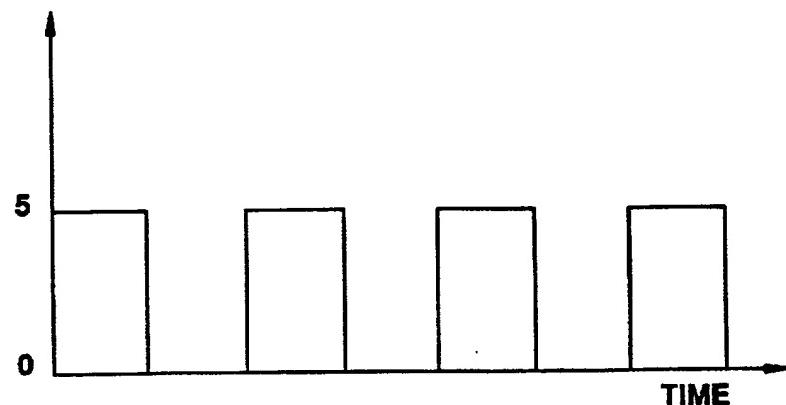


FIG. 9



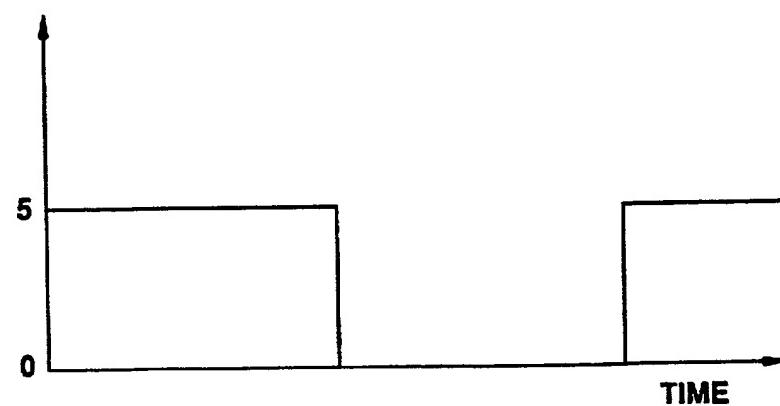
DIGITAL MEMORY
CIRCUIT OUTPUT
VOLTAGE

FIG. 10A



OPPOSITE ELECTRODE
APPLYING VOLTAGE

FIG. 10B



LIQUID CRYSTAL
APPLYING VOLTAGE

FIG. 10C

